REMARKS

At the time of the Office Action dated December 18, 2002, claims 1-5 were pending in this application. Of those claims, claims 1-2 and 5 have been rejected and claims 3 and 4 have been withdrawn from consideration pursuant to the provisions of 37 C.F.R. § 1.142(b). Claims 1 and 2 have been amended. Applicant submits that the present Amendment does not generate any new matter issue.

In the fifth enumerated paragraph of the Office Action, the Examiner asserted that in claim 2, line 4, "setting all said dummy pattern should be changed to --setting all dummy patterns--. In response, Applicant has amended claim 5 per Examiner's suggestion.

CLAIMS 1-2 AND 5 ARE REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY ITOU ET AL., U.S. PATENT NO. 5,594,279 (HEREINAFTER ITOU)

In the seventh enumerated paragraph of the Office Action, the Examiner asserted that Itou discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

The present invention is directed to improving the precision of a finished product in which a pattern of metal wiring is formed though the use of exposure. In so doing, a dummy pattern (also referred to as "dummy metal) is formed to fill a space where the wiring would not be typically formed. Then, all dummy patterns are electrically connected to a reference wiring to fix the potential of the dummy patterns.

In contrast, Itou arranges either shield wiring 81 between a ground wire 2 and a semiconductor substrate 7 or a shield reinforcing wiring 91 between the ground wire 2 and channel wiring 6 to prevent the transfer of noise from the semiconductor substrate to a power supply wire or ground wire. To provide shielding of noise from the semiconductor substrate 7, the shield wiring 81 is positioned below the ground wire 2 and arranged solely to cover an area of the semiconductor substrate 7 slightly wider than the ground wire 2. Furthermore, with regard to the shield reinforcing wire 91 preventing noise propagation from the channel wiring 6 to the ground wire 2, Itou does not teach that the shield reinforcing wiring 91 is arranged to prevent areas without wiring on the same layer as the ground wire (see, for example, the area to the left of the ground wire and the area to the right of bonding pad 3 in Fig. 9). Put simply, with Itou, there exists a difference in density in the wiring patterns formed in a same layer.

Although Fig. 9 of Itou is similar to certain ones of the drawings of Applicant's disclosure, the figure of the present application is shown in a simplified section view from one side. However, in contrasting the present invention to that the disclosure of Itou, it is apparent that Itou does not consider the flatness of the wiring layer. Instead, Itou only arranges the shield wiring to extend adjacent to and parallel to the ground wire and the power supply wire. In contrast, the present invention arranges many dummy patterns in void areas of each wiring layer, thereby filling up the space so as not to leave a thin portion and to maintain a consistent density. Thus, the structure of the present invention is different from that disclosed by Itou.

As a way to show the difference between Itou and the claimed invention, Applicant has appended hereto Figs. 3 and 300 and Figs. 9 and 900. Figs. 3 and 9 correspond to Figs. 3 and 9 disclosed by Itou, and Figs. 300 and 900 disclose the present invention, as applied to Figs. 3 and 9 of Itou. In Fig. 3, the wiring in the uppermost layer and the wiring in the layer immediately below the uppermost layer are shown. the wiring in the uppermost layer is shown by reference numerals 3, 12-16, 24-25, and 27-30. The wiring in the layer immediately below the uppermost layer is shown by reference numerals 2, 11, and 51-54.

When the present invention is applied to Fig. 3 of Itou, dummy patterns will be arranged in the void areas of each layer to provide the structure shown in Fig. 300. The dummy pattern that would be arranged in the uppermost layer is shown as the hatched area of left-up slant lines, and the dummy pattern that would be arranged in the layer below is shown as the hatched area of right-up slant lines. Although a part of the dummy pattern in this layer cannot be seen below the dummy pattern of the uppermost layer, the pattern extends into the unseen area. The present invention is also a structure where the dummy patterns are arranged and electrically connected to the reference wiring to fix the potential of the dummy patterns. As shown from the comparison of Fig. 3 and Fig. 300, the structure of Itou and the invention is different.

Referring to attached Figs. 9 and 900, the purpose in Fig. 9 of Itou is to shield ground wire 2 from noise. However, no wiring is provided in other areas, for example, between in a region immediately below the bonding pad 3 and between ground wire 2 and shield wiring 81. If the present invention is applied to this structure, the structure shown in Fig. 900 would result. The regions shown as the hatched area in Fig. 900 is the dummy patterns and the contacts

electrically connect the dummy patterns with each other. All the dummy patterns are electrically connected to ground wire 2. As bonding wire 3 is connected to ground Vss via wiring 8, dummy patterns are also connected to bonding pad 3. As shown in Fig. 900, the void area of each layer in the multi-layered wiring section is thoroughly filled with dummy patterns to provide a structure without a thin portion. As shown from the comparison of Fig. 9 and Fig. 900, the structure of Itou and the invention is different.

Amended claim 1 recites "said first layer and said second layer include a dummy pattern, each arranged to alleviate for a difference in density in a planar layout of wiring pattern in a same layer." As discussed above, the structure of Itou does not alleviate a difference in density of the wiring pattern formed in a same layer. Thus, Itou fails to identically describe the claimed invention within the meaning of 35 U.S.C. § 102.

Claim 2, dependent upon claim 1, is patentable over Itou at least on the basis of that dependency. Furthermore, with regard to the Examiner's arguments found in the last portion of page 4, upon reviewing M.P.E.P. § 2113, it is clear that the Examiner has misapplied the law with regard to product-by-process limitations. The law provides that product-by-process limitation must be considered by the Examiner in making a determination of novelty or obviousness. Although the Examiner has a reduced burden of proof with regard to product-by-process claims, as discussed in M.P.E.P. § 2113, the Examiner must first provide a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art.[1] However, even if the Examiner

[1] "Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art product." M.P.E.P. § 2113 (citing In re Marosi, 218 USPQ 289 (Fed. Cir. 1983)).

makes this reasoned argument, Applicant has an opportunity to provide evidence that establishes a difference between the product of the prior art and the claimed product.

The Examiner, however, has failed to make any reasoned argument as to why the semiconductor device formed by the process recited in claim 2 is identical to semiconductor device disclosed by Itou. The Examiner has merely asserted that the claimed process and the disclosed process are the same without providing any rationale to support this assertion. Thus, even though the Examiner may have a reduced burden of proof with regard to product-by-process limitations, the Examiner has failed to meet this burden of proof. Therefore, the Examiner has failed to meet the requirements established by the case law and M.P.E.P. § 2113 regarding product-by-process limitations.

With regard to claim 5, Applicant notes that claim 5 is directed to a "designing device" (i.e., a computer). Itou, however, neither teaches nor suggest a designing device. As such, Itou fails to identically disclose the claimed invention, as recited in claim 5, within the meaning of 35 U.S.C. § 102. Applicant, therefore, respectfully submits that the imposed rejection of claims 1-2 and 5 under 35 U.S.C. § 102 for lack of novelty as evidenced by Itou is not factually viable and, hence, solicit withdrawal thereof.

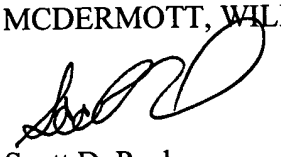
Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing

remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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